

## Product Features

- Support 25.78Gb/s and 10.3Gb/s bi-directional data links
- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8432 and SFF-8472
- Build-in CDR with 25.78Gb/s operation
- SFP28 MSA package with duplex LC connector
- Uncooled 850nm VCSEL Laser
- Single +3.3V power supply
- Class 1 laser safety certified
- Metal enclosure, for lower EMI
- Commercial operating temperature: 0°C to +70°C
- Up to 70m on OM3 MMF and 100m on OM4 MMF
- RoHS Compliant



## Applications

- High speed storage area networks
- 25G high speed interconnection
- 10G Ethernet 10GBASE-SR/SW
- Support CPRI rate: 24.3Gb/s

## Ordering Information

**Table 1. Ordering Information**

Part Number	Transmitter	Output Power	Receiver	Sensitivity	Reach	Temp	DDM	RoHS
LX6501CDH	850nm VCSEL	-7.6 ~ +2.4dBm	PIN	<-10.3dBm	OM4:100m OM3:70m	0 ~ 70 °C	Available	Compliant

## Descriptions

LX6501CDH SFP28 transceivers, according to 25Gigabit Small Form Factor Pluggable “SFP28” Multi-Sourcing Agreement (MSA) SFF-8431 Rev. 4.1 and SFF-8472 Rev.12.1, are designed for use up to 25.78Gb/s data rate over multimode fiber. They are compatible with SFF-8432.

## Pin Description

**Table 2. Pin Description**

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Rate Select 0 – Not used, Presents high input impedance	6
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	Rate Select 1 – Not used, Presents high input impedance	6
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O), AC Coupled	-
13	RD+	Received Data out (CML-O), AC Coupled	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I), AC Coupled	-
19	TD-	Inverse Transmitter Data In (CML-I), AC Coupled	-
20	VeeT	Transmitter Ground	1

**Notes:**

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to

VccHost.

3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
6. Rate select can also be set through the 2-wire bus in accordance with SFF-8472 v. 10.2, Rx Rate Select is set at Bit 3, Byte 110, Address A2h. Tx Rate Select is set at Bit 3, Byte 118, Address A2h.

Note: writing a “1” selects maximum bandwidth operation. Rate select is the logic OR of the input state of Rate Select Pin and 2-wire bus.

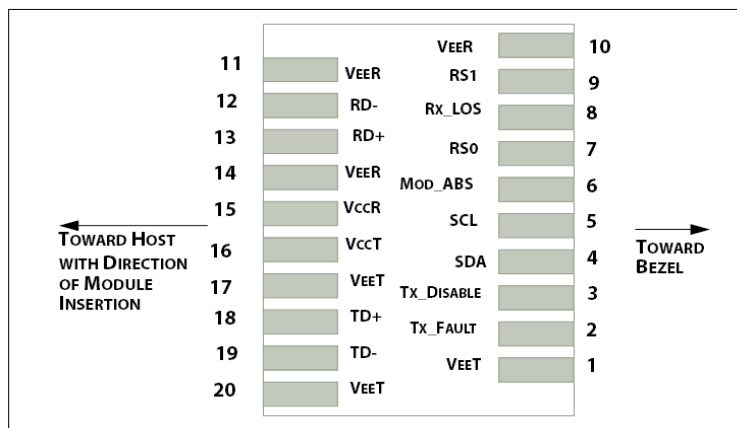


Figure 1. Host PCB SFP+ pad assignment top view

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T <sub>s</sub>	-40	85	°C
Relative Humidity	RH	5	85	%
Supply Voltage	V <sub>cc</sub>	-0.5	4.0	V

## Recommended Operating Conditions

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T <sub>c</sub>	0	25	70	°C
Supply Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V
Data Rate	-	-	25.78	-	Gb/s

## Transceiver Electrical Characteristics

**Table 5. Transceiver Electrical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes	
Module Supply Current	I <sub>cc</sub>	-	-	290	mA	-	
Power Dissipation	P <sub>D</sub>	-	-	1000	mW	-	
<b>Transmitter</b>							
Input Differential Impedance	Z <sub>IN</sub>	-	100	-	Ω	-	
Differential Data Input Swing	V <sub>IN, P-P</sub>	180	-	700	mV <sub>P-P</sub>	-	
TX_FAULT	Transmitter Fault	V <sub>OH</sub>	2.0	-	V <sub>cc</sub>	V	-
	Normal Operation	V <sub>OL</sub>	0	-	0.8	V	-
TX_DISABLE	Transmitter Disable	V <sub>IH</sub>	2.0	-	V <sub>cc</sub>	V	-
	Transmitter Enable	V <sub>IL</sub>	0	-	0.8	V	-
<b>Receiver</b>							
Output Differential Impedance	Z <sub>O</sub>	-	100	-	Ω	-	
Differential Data Output Swing	V <sub>OUT, P-P</sub>	300	-	850	mV <sub>P-P</sub>	1	
Data Output Rise Time, Fall Time	t <sub>r</sub> , t <sub>f</sub>	-	30	-	ps	2	
RX_LOS	Loss of signal (LOS)	V <sub>OH</sub>	2.0	-	V <sub>cc</sub>	V	3
	Normal Operation	V <sub>OL</sub>	0	-	0.8	V	-

**Notes:**

1. Internally AC coupled, but requires an external 100Ω differential load termination.
2. 20–80%.
3. LOS is an open collector output. Should be pulled up with 4.7KΩ on the host board.

## Transmitter Optical Characteristics

**Table 6. Transmitter Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Launch Optical Power	P <sub>o</sub>	-7.6	-	+2.4	dBm	1
Tx Power (OMA)	P <sub>oma</sub>	-4	-	-	dBm	1
Extinction Ratio	ER	2	-	-	dB	
Center Wavelength Range	λ <sub>c</sub>	840	850	860	nm	-
Transmitter Dispersion Penalty @25.78Gb/s	TWDP	-	-	4.3	dB	
Spectral Width (RMS) @25.78Gb/s	Δλ	-	-	0.6	nm	-
Optical Return Loss Tolerance	ORLT	-	-	12	dB	-
P <sub>out</sub> @TX-Disable Asserted	P <sub>off</sub>	-	-	-30	dBm	1

**Notes:**

1. 50/125μm fiber with NA = 0.2.

## Receiver Optical Characteristics

**Table 7. Receiver Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Center Wavelength	λ <sub>c</sub>	840	-	860	nm	-
Receiver Sensitivity (P <sub>avg</sub> )	S	-	-	-10.3	dBm	1
Receiver Overload (P <sub>avg</sub> )	P <sub>OL</sub>	2.5	-	-	dBm	
Optical Return Loss	ORL	12	-	-	dB	-
LOS De-Assert	LOS <sub>D</sub>	-	-	-11	dBm	-
LOS Assert	LOS <sub>A</sub>	-30	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

**Notes:**

1. Measured with PRBS 2<sup>31</sup>-1 at 5e-5 BER @25.78Gb/s.

## Digital Diagnostic Memory Map

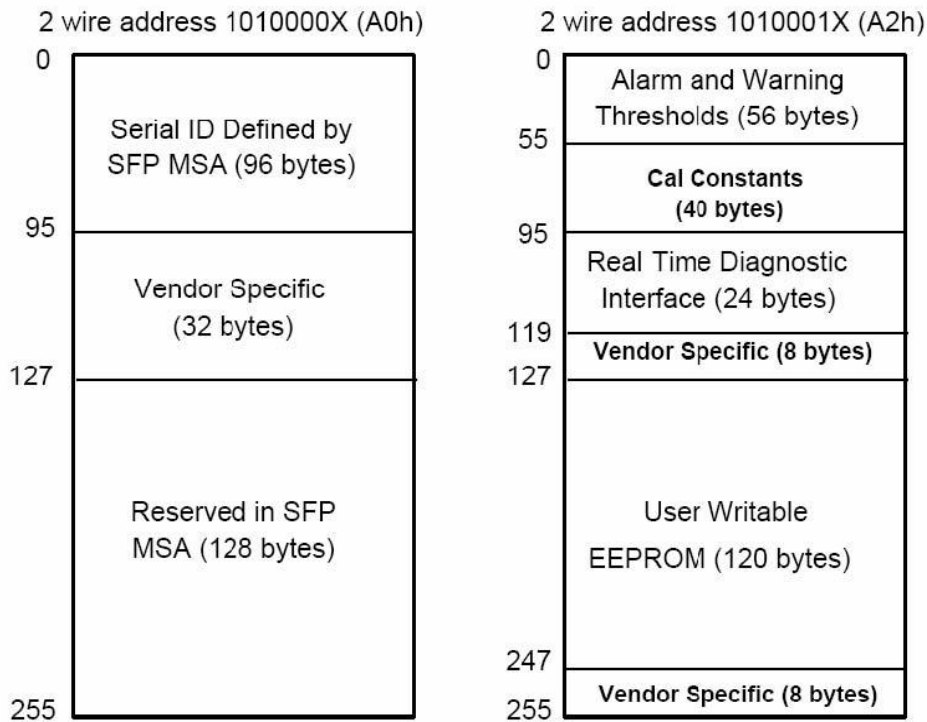


Figure 2. Digital Diagnostic Memory Map Specific Data Field Descriptions

## EEPROM Serial ID Memory Contents

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h), and the clock frequency up to 100 KHz. The memory contents are shown in Table 8.

**Table 8. Serial ID Memory Contents**

A0 LOW EEPROM Definition

Data Address	Name of Field	Contents(Hex)	Description
0	Identifier	03	SFP28
1	Ext. Identifier	04	SFP28 function is defined by serial ID

2	Connector	07	LC
3-10	Transceiver	00 00 00 00 00 00 00 00	
11	Encoding	06	64B/66B
12	BR, Nominal	FF	25.78Gb/s
13	Rate Identifier	00	
14	Length (9µm) km	00	-
15	Length (9µm) 100m	00	-
16	Length (50µm) 10m	00	-
17	Length(62.5µm)10m	00	-
18	Length (OM4) 10m	0A	100m
19	Length (50µm OM3) 10m	07	70m
20-35	Vendor name	4C 49 4E 4B 54 45 4C 20 20 20 20 20 20 20 20 20	LINKTEL (ASCII)
36	Extended Specific	02	25G Base-SR
37-39	Vendor OUI	68 E8 EB	
40-55	Vendor PN	4C 58 36 35 30 31 43 44 48 20 20 20 20 20 20 20	"LX6501CDH" (ASCII)
56-59	Vendor rev	31 2E 30 20	Rev 1.0 ( ASCII)
60-62	Wavelength	03 52 00	850nm
63	CC BASE	xx	Check sum of bytes 0 - 62
64-65	Options	18 3A	LOS, TX_FAULT and TX_DISABLE
66	BR, max	67	25.78Gb/s
67	BR, min	00	
68-83	Vendor SN	33 31 34 30 31 30 31 30 30 31 20 20 20 20 20 20	Serial Number of transceiver (ASCII). For example "3140101001" .
84-91	Vendor date code	xx xx xx xx xx xx 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes)
92	Diagnostic type	68	Diagnostics (Internally Cal)
93	Enhanced option	F8	Diagnostics(Optional Alarm/warning flags, Soft TX_DIS, Soft TX_FAULT and Soft TX_LOS monitoring)
94	SFF-8472	08	Diagnostics(SFF-8472 Rev 12.0)
95	CC_EXT	xx	Check sum for bytes 64-94

**Note:** The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of SFF-8472 Rev 12.0.

A2 LOW EEPROM Definition

Data Address	Name of Fields	Contents(Hex)	Description
0-1	Temp High Alarm	4B 00	Set to 75°C
2-3	Temp Low Alarm	F6 00	Set to -10°C
4-5	Temp High Warning	46 00	Set to 70°C
6-7	Temp Low Warning	FB 00	Set to -5°C
8-9	Voltage High Alarm	8C A0	Set to 3.60V
10-11	Voltage Low Alarm	71 48	Set to 2.90V
12-13	Voltage High Warning	88 B8	Set to 3.50V
14-15	Voltage Low Warning	75 30	Set to 3.00V
16-17	Bias High Alarm	1B 58	Set to 14mA
18-19	Bias Low Alarm	03 E8	Set to 2mA
20-21	Bias High Warning	19 64	Set to 13mA
22-23	Bias Low Warning	05 DC	Set to 3mA
24-25	TX Power High Alarm	55 76	Set to 3.4dBm
26-27	TX Power Low Alarm	05 64	Set to -8.6dBm
28-29	TXPower High Warning	43 E2	Set to 2.4dBm
30-31	TX Power Low Warning	06 CA	Set to -7.6dBm
32-33	Rx Power High Alarm	55 76	Set to 3.4dBm
34-35	Rx Power Low Alarm	02 E6	Set to -11.3dBm
36-37	Rx Power High Warning	43 E2	Set to 2.4dBm
38-39	Rx Power Low Warning	03 A6	Set to -10.3dBm

## Diagnostic Monitor Specifications

The digital diagnostic monitoring interface also defines another 256-byte memory map in EEPROM, which makes use of the 8 bit address 1010001X (A2h). Please see Figure 2. For detail EEPROM information, please refer to the related document of SFF-8472 Rev 12.0. The monitoring specification of this product is described in Table 9.

**Table 9. Diagnostic Monitor Specifications**

Parameter	Range	Accuracy	Calibration
Temperature	-10 to +75°C	±3°C	Internal
Voltage	2.9 to 3.6V	±3%	Internal



Bias Current	2 to 14mA	±10%	Internal
TX Power	-8.6 to 3.4dBm	±3dB	Internal
RX Power	-11.3 to 3.4dBm	±3dB	Internal

## Recommended Host Board Power Supply Filter Network

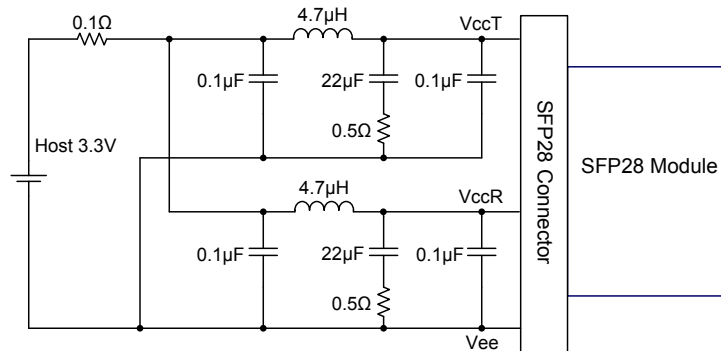


Figure 3. Recommended Host Board Power Supply Filter Network

## Recommended Application Interface Block Diagram

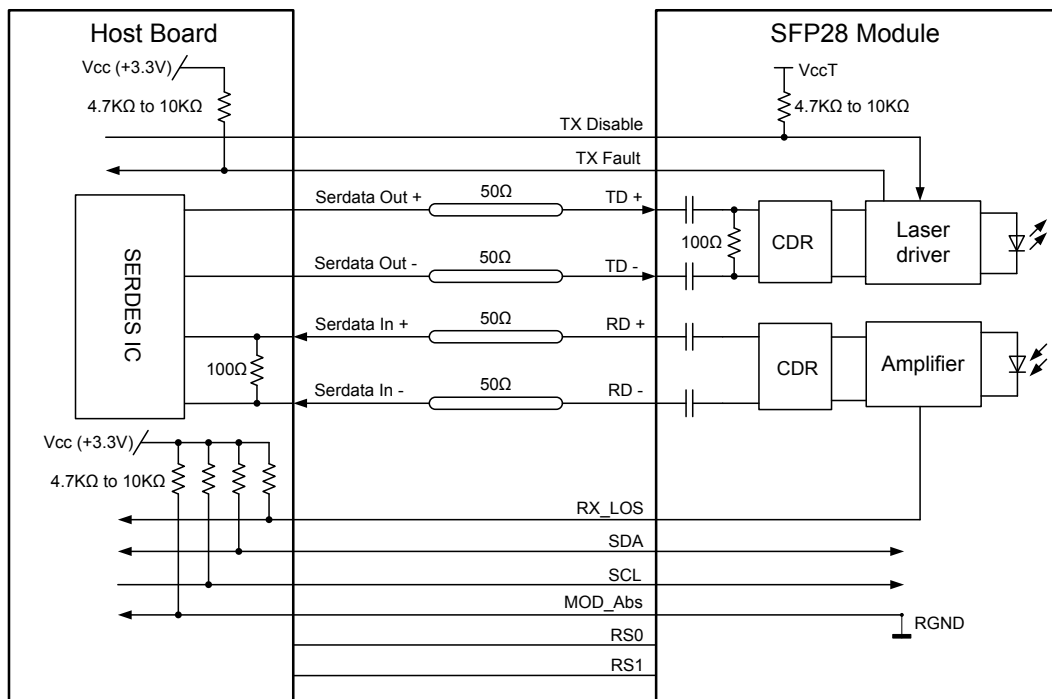


Figure 4. Recommended Application Interface Block Diagram

## Mechanical specifications

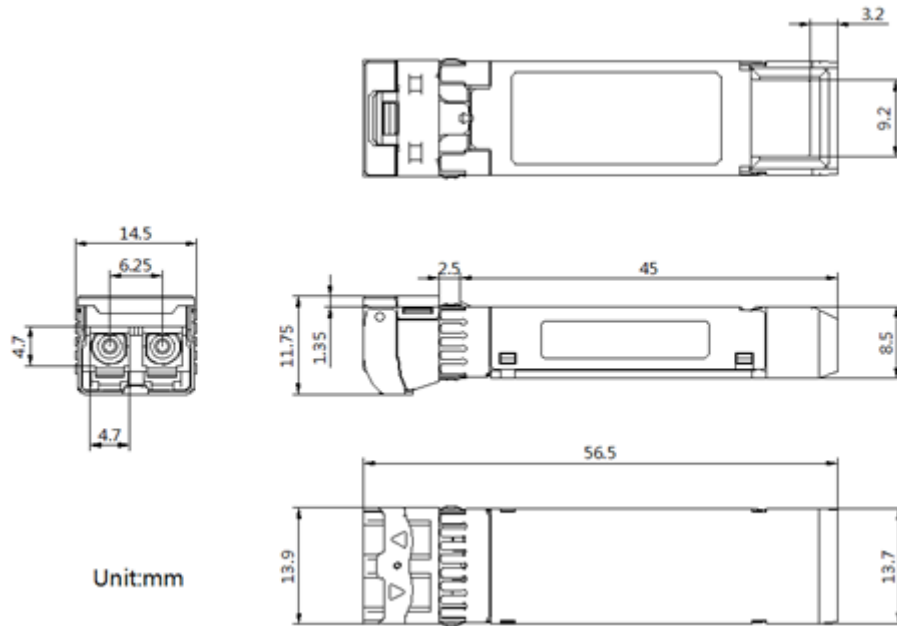


Figure 5. Outline Drawing

## PCB layout recommendation

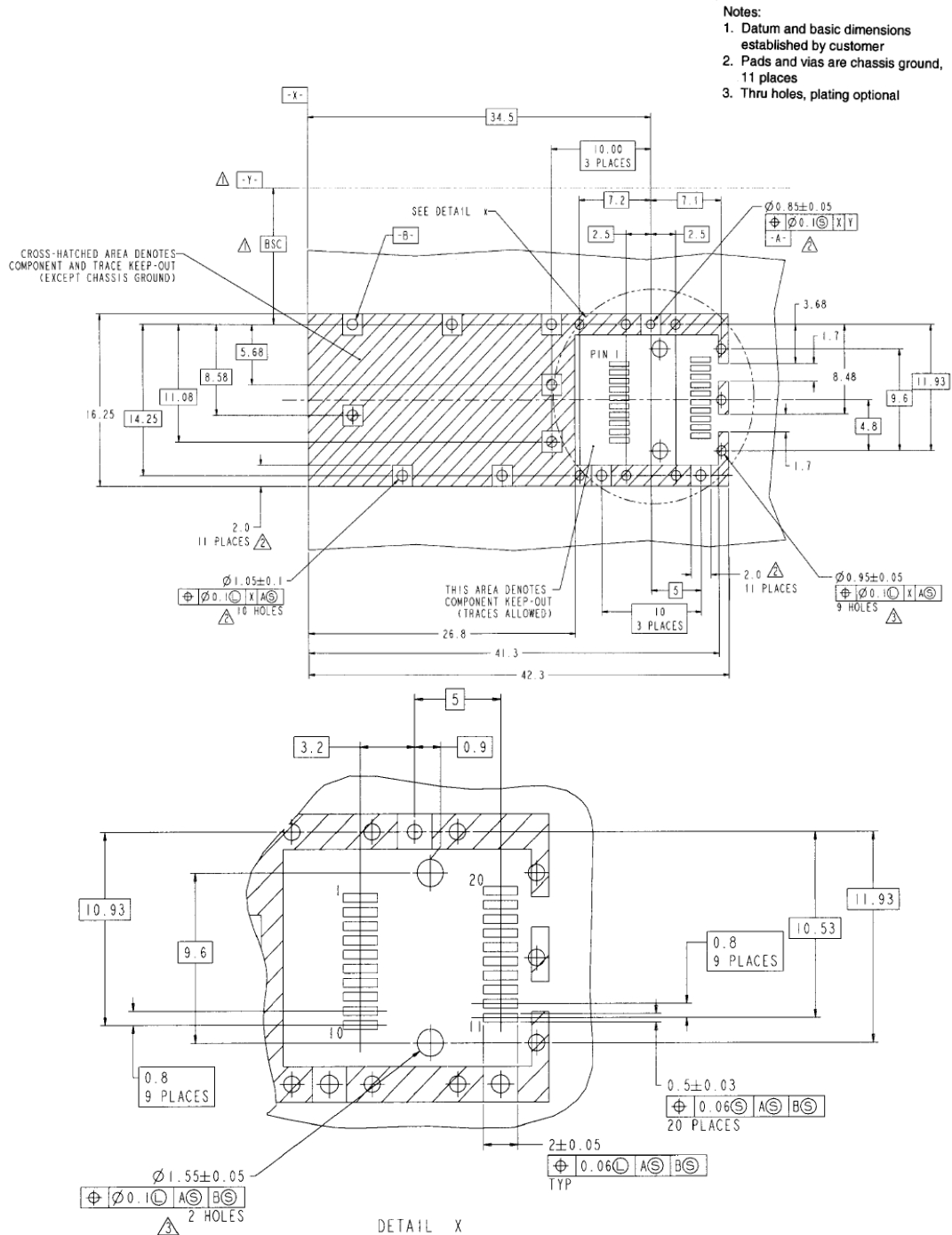


Figure 6. PCB layout recommendation

## Revision History

<b>Date</b>	<b>Rev</b>	<b>Description</b>	<b>Modified By</b>
07/25/2019	V1.0	Preliminary Release	Junyi Wu
02/22/2023	V1.1	The domain name is updated to .linktel.com	Wei Chen

## For More Information

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