

## Product Features

- Compliant to industrial standard SFP MSA
- High speed / high density: support up to 10 Gb/s bi-directional operation.
- Reliable VCSEL and PIN photonic devices
- I2C standard management interface
- Excellent high speed signal integrity
- Operating temperature Options
  - (Commercial) 0°C to +70°C
- RoHS Compliant



## Applications

- 10G Ethernet
- Proprietary high speed, high density data
- High performance computing, server and data storage.

## Descriptions

LX495xCDR is a 10Gb/s, hot pluggable active optical cable for Ethernet data transmission. It provides full duplex operation and supports distance up to 100 meters.

LX495xCDR is composed of optical transceivers in both ends and multimode fiber cable in between. This integrated optical module solution removes the complicated optical fiber interface and brings friendly and intuitive electrical-to-electrical interface to users.

LX495xCDR is designed to meet the requirements of high speed, high density and low power consumption for applications in today's data centers.

## Ordering Information

Table 1. Ordering Information

Part Number	Reach	Temp	RoHS
LX4951CDR	1m	0 ~ 70 °C	Compliant
LX4952CDR	2m	0 ~ 70 °C	Compliant
LX4953CDR	3m	0 ~ 70 °C	Compliant
LX4954CDR	5m	0 ~ 70 °C	Compliant
LX4955CDR	10m	0 ~ 70 °C	Compliant
LX4956CDR	20m	0 ~ 70 °C	Compliant
LX4957CDR	30m	0 ~ 70 °C	Compliant
LX4958CDR	50m	0 ~ 70 °C	Compliant
LX4959CDR	100m	0 ~ 70 °C	Compliant

## Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Rate Select 0 – Not used, Presents high input impedance	-
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	Rate Select 1 – Not used, Presents high input impedance	-
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	-
13	RD+	Received Data out (CML-O)	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	-
19	TD-	Inverse Transmitter Data In (CML-I)	-
20	VeeT	Transmitter Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7K $\Omega$  to 10K $\Omega$  pull-up resistor to VccHost.

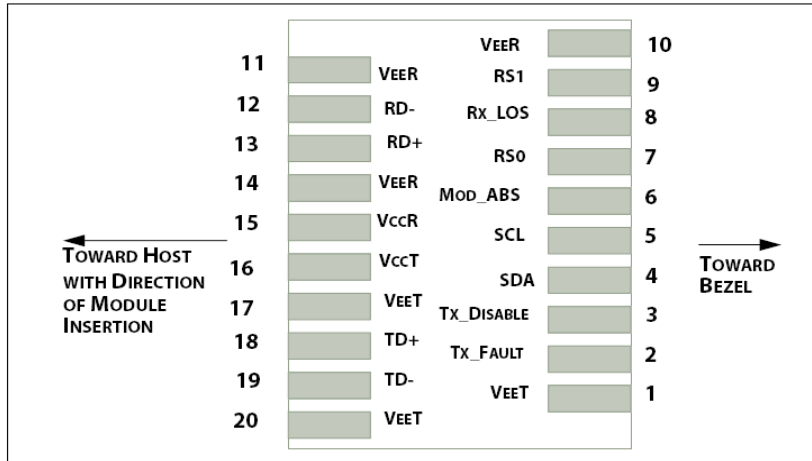


Figure 1. Host PCB SFP+ pad assignment top view

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	Ts	-40	85	°C
Relative Humidity	RH	5	85	%
Supply Voltage	Vcc	0	3.6	V

## Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	LX495xCDR Tc	0	25	70	°C
Supply Voltage	Vcc	3.135	3.3	3.465	V
Data Rate	-	-	10.3	-	Gb/s

## Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
+3.3V Supply Current	I <sub>cc</sub>	-	-	290	mA	-
Power Dissipation	P <sub>D</sub>	-	-	1000	mW	-
Low speed output: Transmitter Fault(TX_FAULT) / Loss of Signal (LOS)	VOH	2.0	-	V <sub>cc</sub>	V	1
	VOL	0	-	0.8	V	1
Low speed input: Transmitter Disable (TX_DISABLE), MOD_DEF 1, MOD_DEF 2	VIH	2.0	-	V <sub>cc</sub>	V	2
	VIL	0	-	0.8	V	2
Clock Rate-I2C	f	-	-	400	kHz	3

Notes:

1. For all control input pins: TX\_DISABLE.
2. For all status output pins: RX\_LOS, TX\_FAULT.
3. For management interface.

## Transmitter Optical Characteristics

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Reference Differential Input Impedance	Z <sub>d</sub>	-	100	-		1
Signal Speed	-	-	10.3	-	Gb/s	2
Differential Data Input Swing	V <sub>in_pp</sub>	180	-	700	mV	-

Notes:

1. AC coupled inside AOC module.
2. Tested with PRBS2<sup>31</sup>-1 BER: 10E<sup>-12</sup>.

## Receiver Optical Characteristics

Table 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Reference Differential Input Impedance	Z <sub>d</sub>	-	100	-		1
Signal Speed	-	-	10.3	-	Gb/s	2
Differential Data Output Swing	-	150	-	850	mV	-
Differential Data Output Swing When Squelched	-	-	-	50	mV	-
Rise / Fall Time (20% ~80%)	-	24	-	-	ps	-

Notes:

1. AC coupled inside AOC module.
2. Tested with PRBS2<sup>31</sup>-1 BER: 10E<sup>-12</sup>

## Recommended Application Interface Circuit

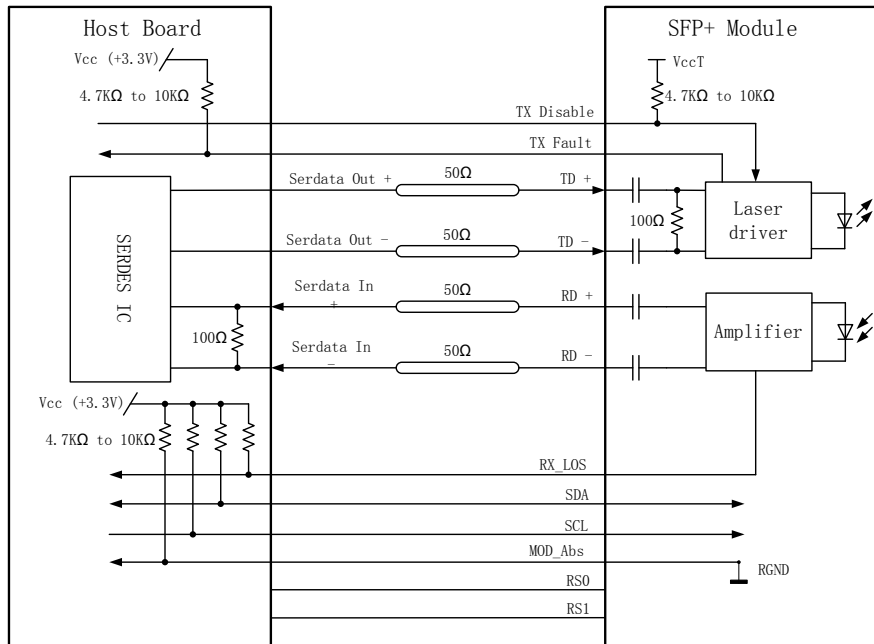


Figure 4. Recommended Application Interface Circuit

## Mechanical specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
AOC cable length (L ≤ 5m)	L	L-0.06	L	L+0.06	M	-
AOC cable length (L > 5m)	L	L-(L*1.1%)	L	L+(L*1.1%)	M	-
Module Retention	-	90	-	170	N	-
Module Insertion	-	0	-	18	N	-
Module Extraction	-	0	-	25	N	-
Cable Pull Strength – Apply Load at 0	-	44	-	-	N	-
Cable Pull Strength – Apply Load at 90	-	33	-	-	N	-
Clearance Out of IO Bezel	-	75	-	-	nm	-
Cable Bending Radius	-	30	-	-	nm	-
Insertion / Removal Cycles	-	50	-	-	cycles	-

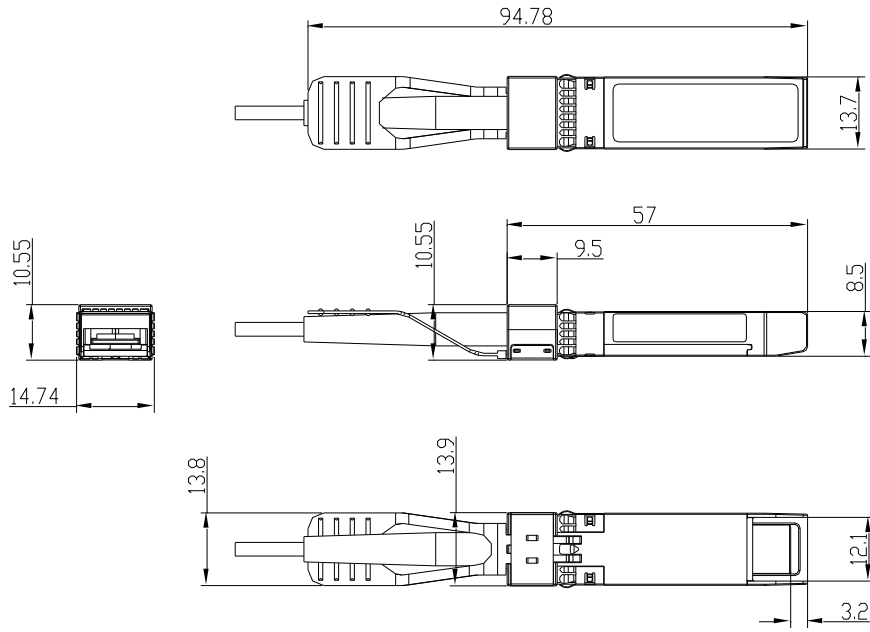


Figure 5. Outline Drawing

## PCB layout recommendation

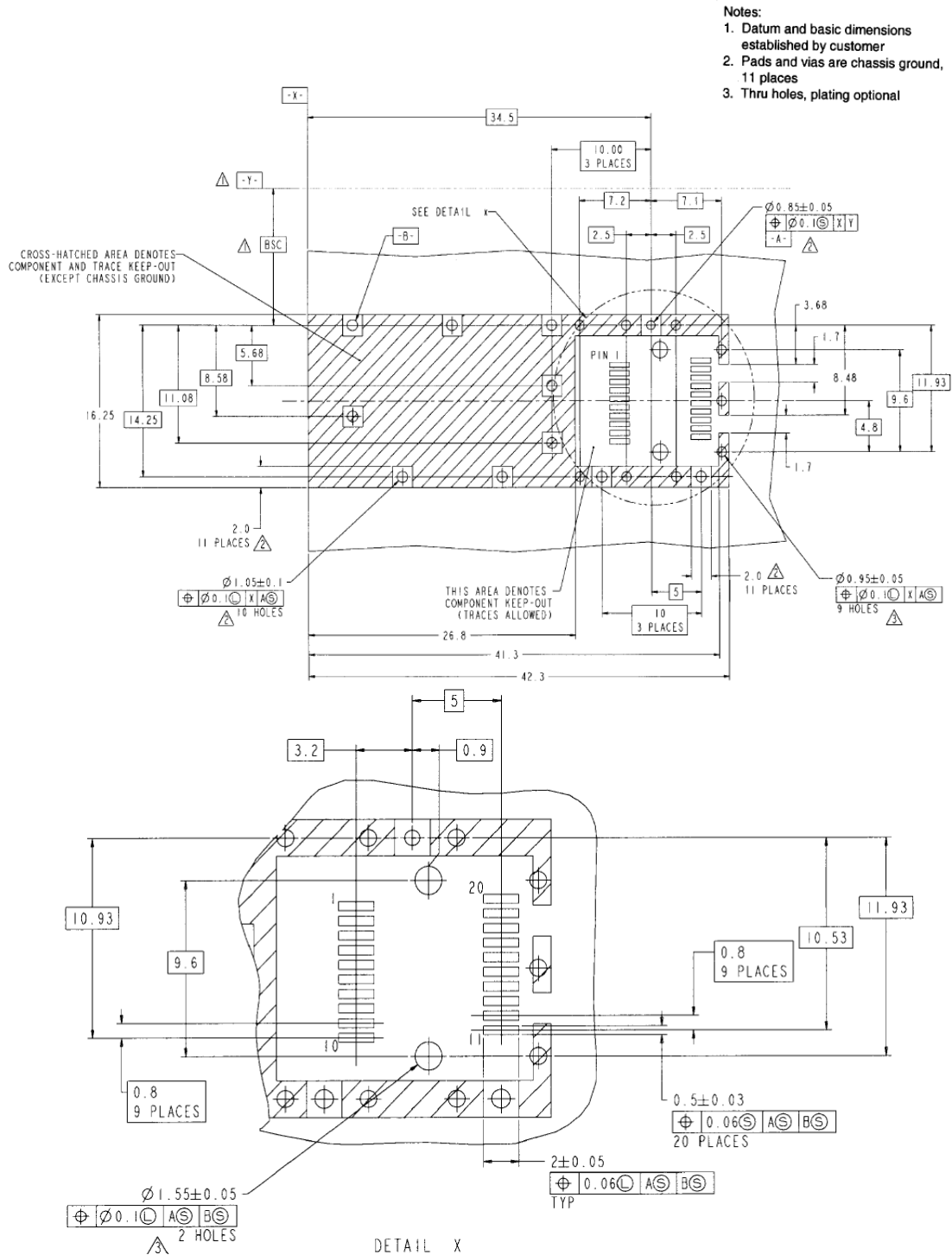


Figure 6. PCB layout recommendation

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## For More Information

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